D. Sebastian Heredia

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Electrical engineer specializing in embedded systems, robotics, and FPGA-accelerated hardware, with hands-on experience in digital design, control systems, and hardware-software integration for real-time applications.

EDUCATION

Harvey Mudd College, Claremont, CA *Exp. Grad. May 2027*

- *B.S. Engineering, GPA: 3.51 / 4.00, Dean's List*
- *Activities:* Mudd Amateur Rocketry Club, Division-III Ultimate Frisbee, SALSA Mudd

Selected Coursework

- Microprocessor Systems, Digital Electronics & Computer Architecture, Signals & Systems, Control Systems, Manufacturing & Design, Mechanical Design, Applied Mathematics for Engineers, Experimental Engineering, Engineering Clinic Program

PROJECTS

Instrument Tuner Integrating FFT on FPGA, *Microprocessor Systems: Design & Application* *Oct. 2025 - Dec. 2025*

- Built a real-time pitch detection system to enable low-latency, high-precision audio analysis on resource-constrained hardware.
- Implemented a 512-point fixed-point FFT on FPGA, achieving sub-Hz frequency resolution without floating-point hardware.
- Demonstrated how FPGA acceleration can outperform MCU-only solutions for real-time signal processing.

Harvey Mudd College Clinic Project (Apple Inc.), *Fall Clinic I Engineering (NDA)* *Aug. 2025 - Dec. 2025*

- Conducted R&D towards an automated polishing system to reduce variability in cosmetic manufacturing processes.
- Improved surface finish consistency and production yield, addressing manufacturing bottlenecks in elastomeric component fabrication.
- Contributed to automation strategy for scaling high-precision finishing in industrial settings.

Autonomous Surface Vehicle (ASV), *Experimental Engineering* *Jan. 2025 - April 2025*

- Designed a low-cost autonomous sensing platform for shallow-water mapping (<$50 total system cost).
- Fused data from Hall-effect, pressure, and motor-based sensors to improve robustness to noise and sensor failure.
- Validated that low-cost systems can achieve high-resolution bathymetric mapping comparable to commercial equipment.

32-Bit Multicycle Computer Processor (RISC-V), *Digital Electronics & Computer Architecture* *Sept. 2024 - Dec. 2024*

- Designed and implemented a 32-bit multicycle RISC-V processor in SystemVerilog including datapath, ALU, register file, and control FSM, exploring tradeoffs between performance and hardware complexity.
- Verified instruction execution through waveform-level debugging, ensuring correct control sequence and data path timing.

WORK EXPERIENCE

Engineering Course Staff, *TA, Mentor, Writing Proctor,* Claremont, CA *Sept. 2025 - Present*

- Led tutorials and mentoring sessions for 100+ students across core engineering courses (E72, E79, E80).
- Taught analytical modeling of linear time-invariant systems and supported MATLAB-based problem solving.
- Provided structured feedback on technical writing, lab reports, and experimental methodology.

Harvey Mudd College Machine Shop, *Shop Proctor,* Claremont, CA *Sept. 2024 - Present*

- Taught 100+ first-time users each semester how to use the metal shop and wood shop equipment safely to prevent injury.
- Provided users with on-the-spot guidance to improve machining techniques, fostering confidence and competence.

Department of Medicine Statistics Core (DOMStat) at UCLA, *Student Assistant*, Westwood, CA *Aug. 2024 - Present*

- Designed and tested a REDCap database to streamline proposal tracking for 80+ Department of Medicine PIs.
- Developed a user-focused DOMStat website interface emphasizing accessibility and information architecture.

SKILLS

- **Hardware / FPGA:** SystemVerilog, FPGA Design, Fixed-Point DSP, Lattice Radiant, Quartus, Questa
- **Embedded / Programming:** C, Python, MATLAB / Simulink, Arduino
- **Design & CAD:** KiCad, EAGLE, SolidWorks, COMSOL
- **Lab & Machining:** Oscilloscope, SMT Soldering, CNC Mill, Lathe, Laser Cutter, 3D Printer
- **Other:** GitHub, REDCap, MS Office, Spanish (Native / Fluent), California Seal of Biliteracy in Spanish